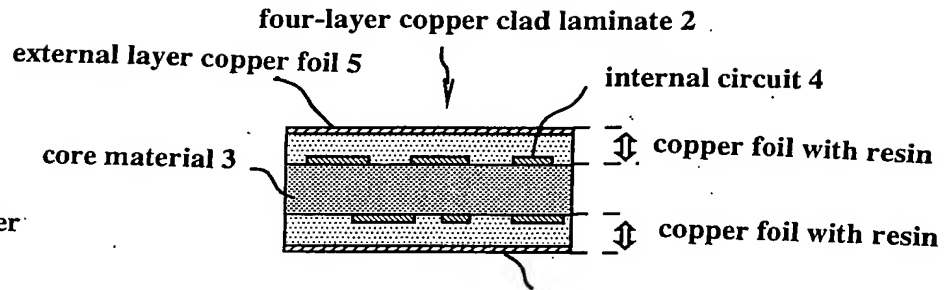


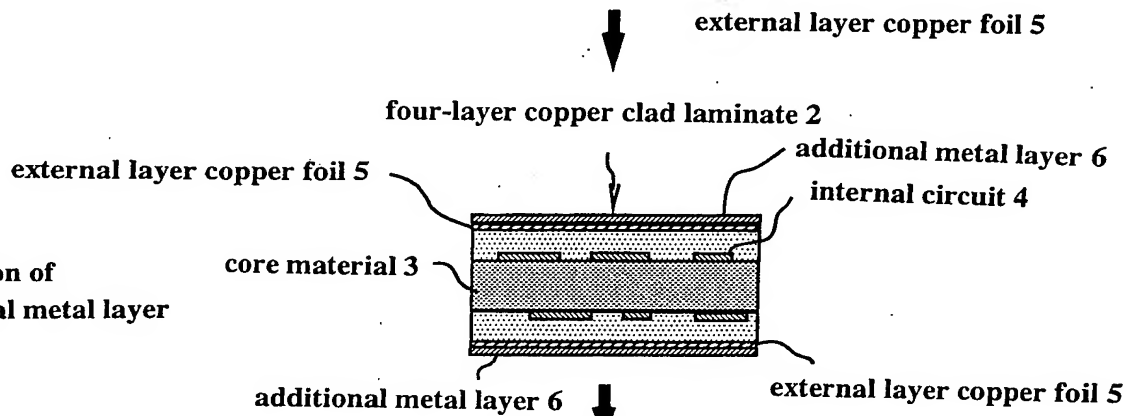
FIG. 1



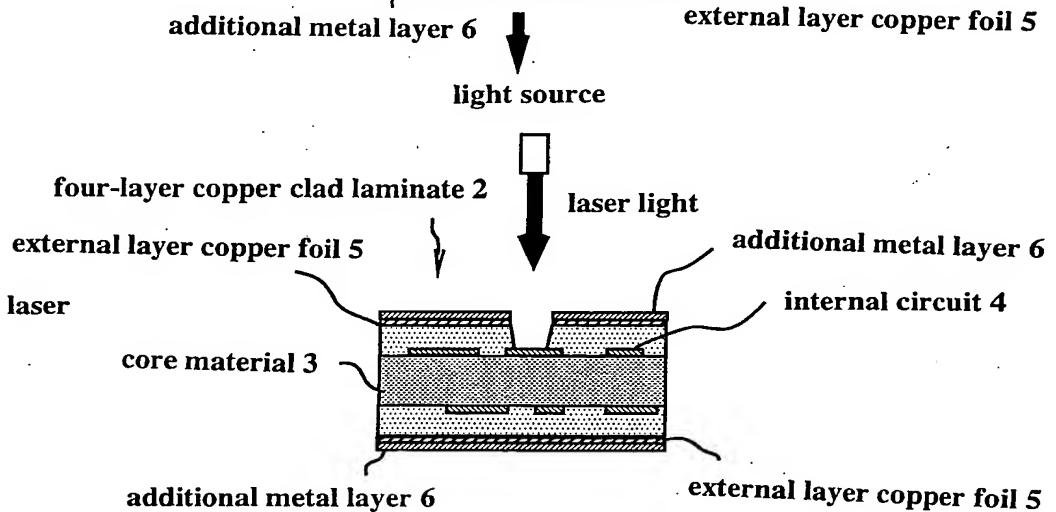
(a) Manufacture of four-layer copper clad laminate



(b) Formation of additional metal layer



(c) Hole-drilling by laser



(d) Peeling-off of an additional metal layer

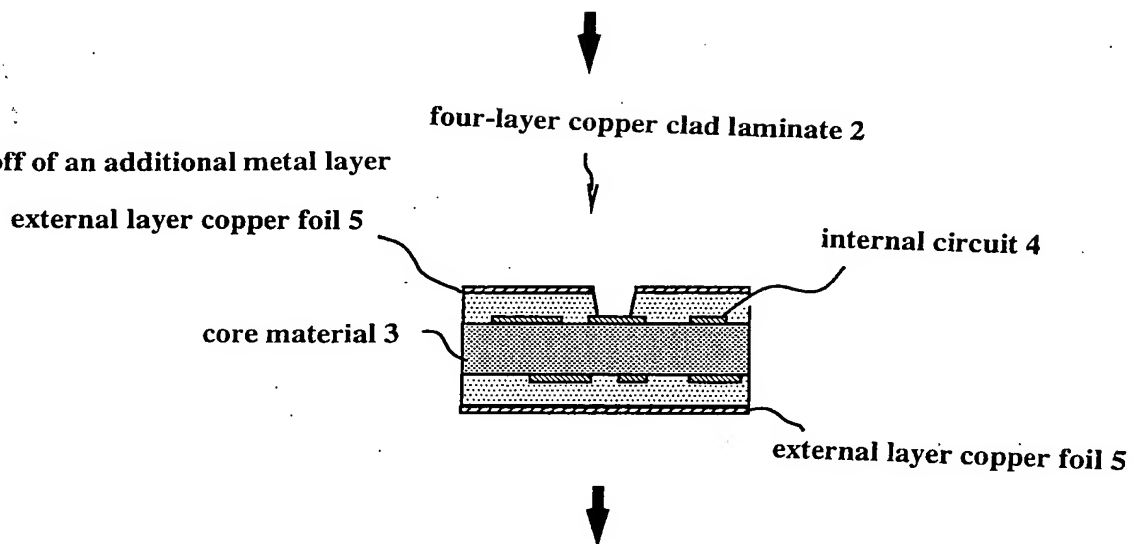


FIG. 2



(e) Formation of
plated copper layer

four-layer copper clad laminate 2
plated copper layer 7

external layer copper foil 5

internal circuit 4

core material 3

external layer copper foil 5

plated copper layer 7

(f) Formation of
etching resist layer

four-layer copper clad laminate 2

plated copper layer 7

etching resist layer 8

external layer copper foil 5

internal circuit 4

core material 3

plated copper layer 7

external layer copper foil 5

etching resist layer 8

(g) Exposure and development

four-layer copper clad laminate 2

plated copper layer 7

etching resist layer 8

external layer copper foil 5

internal circuit 4

core material 3

plated copper layer 7

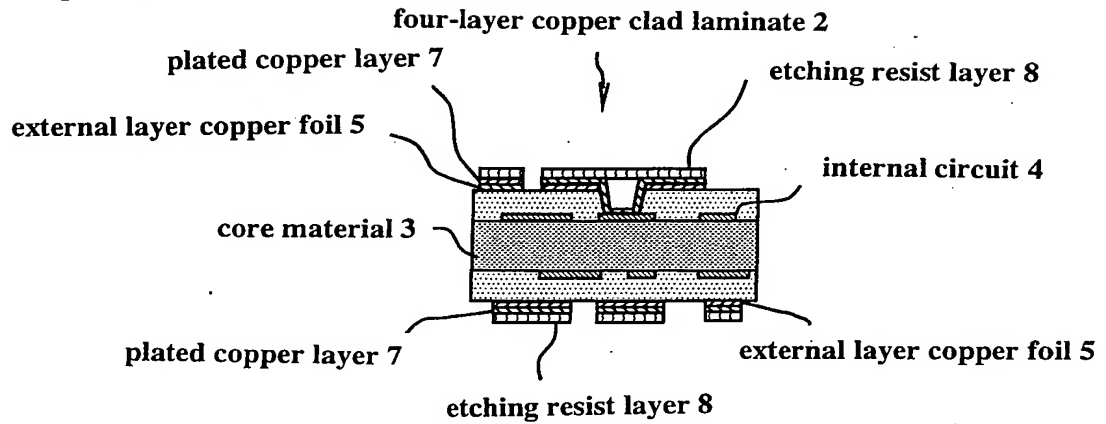
external layer copper foil 5

etching resist layer 8

FIG. 3



(h) Formation of a circuit
through etching



(i) Peeling-off of
etching resist layer

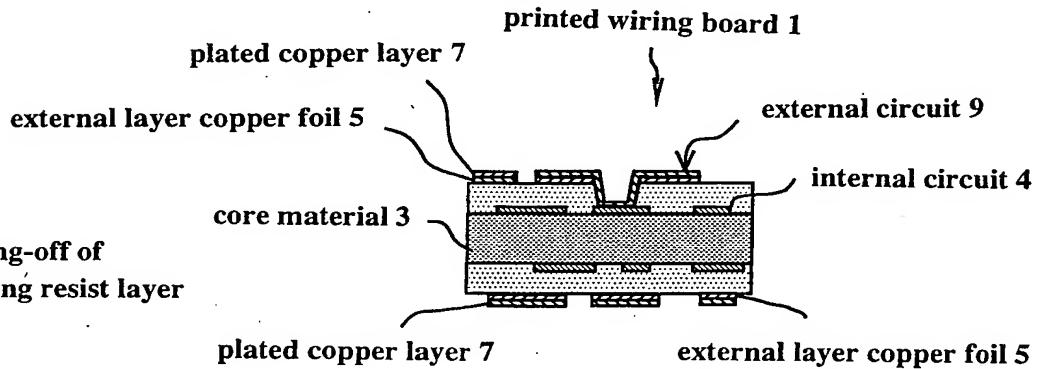


FIG. 4

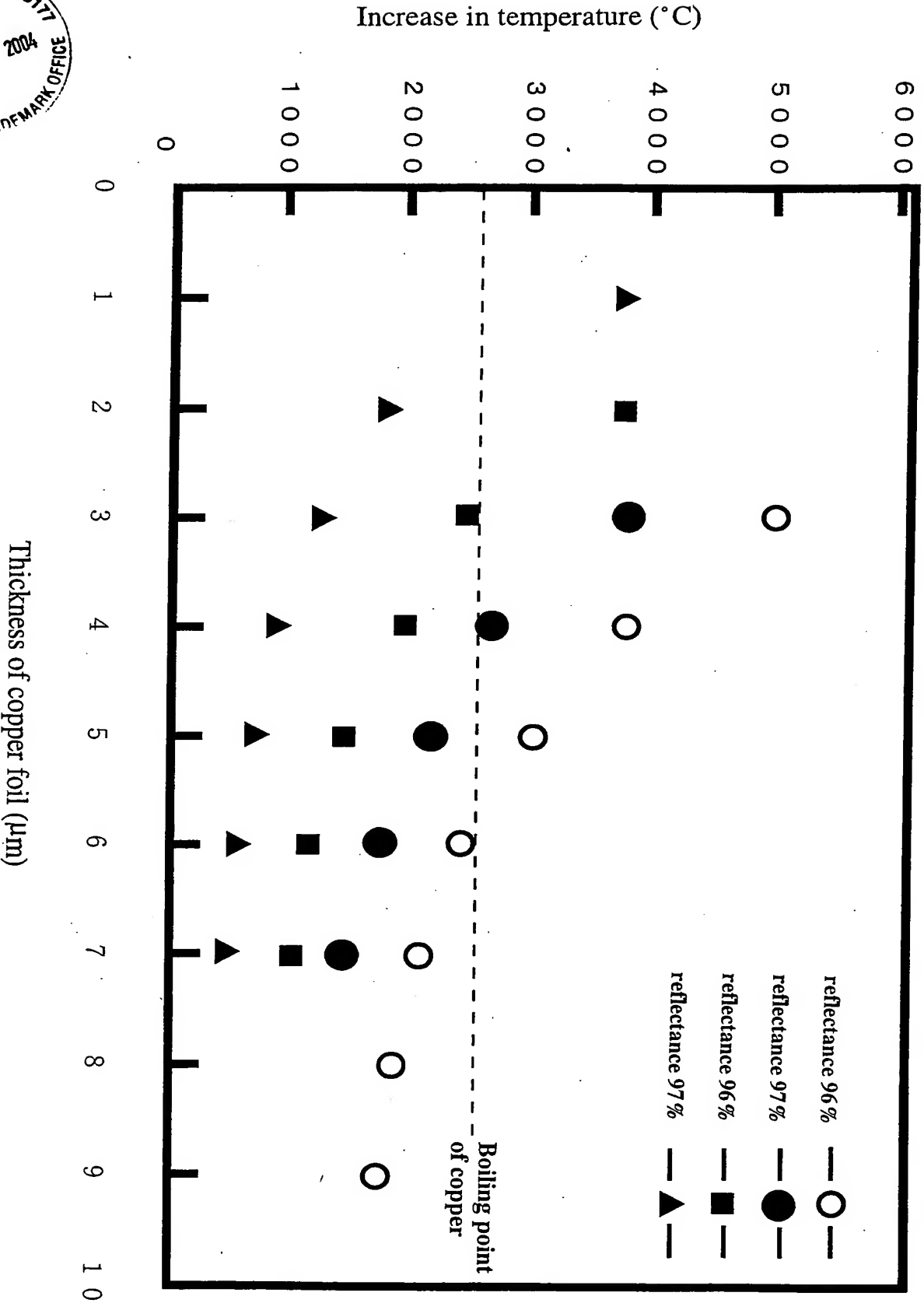


FIG. 5

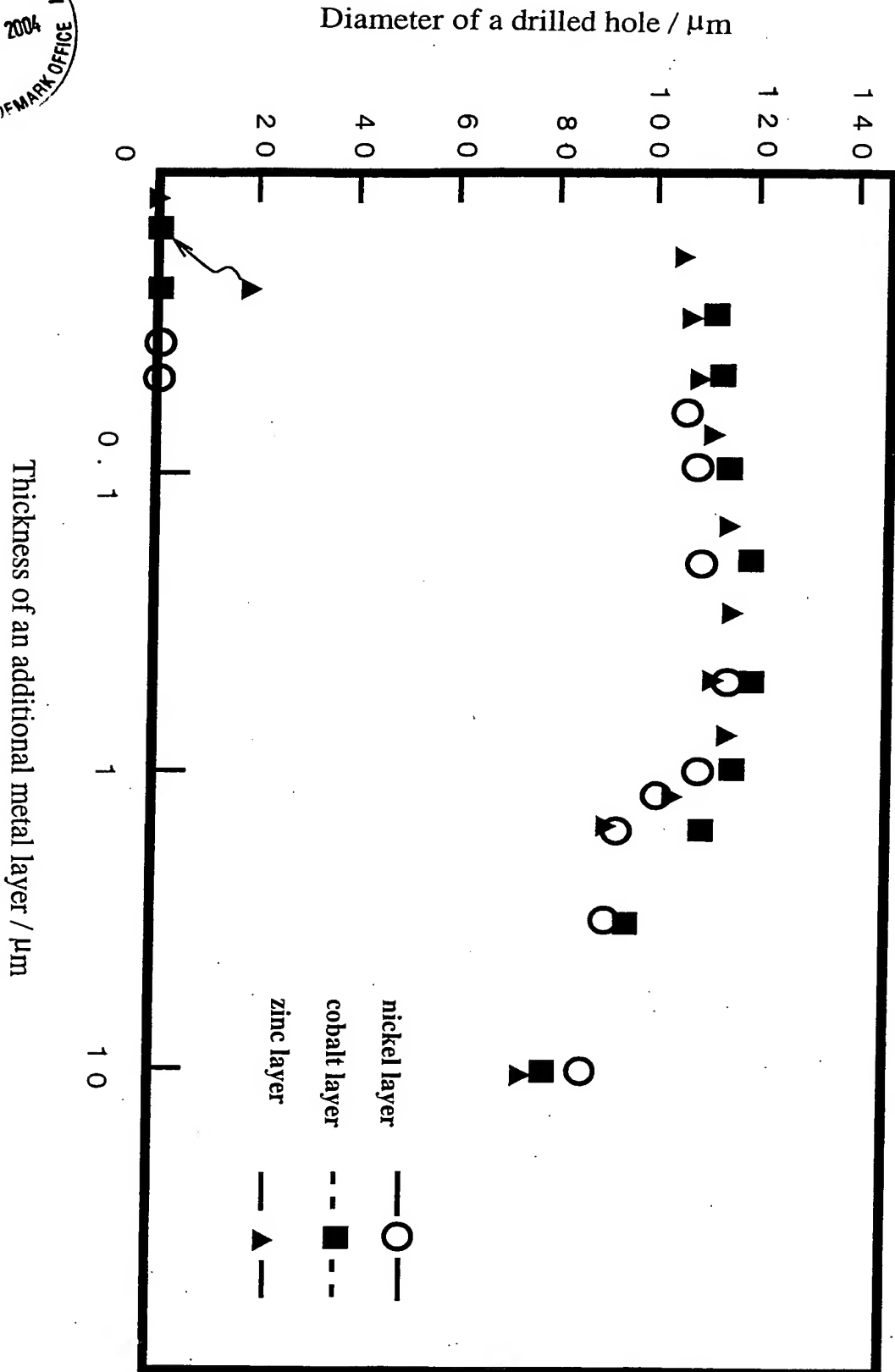


FIG. 6

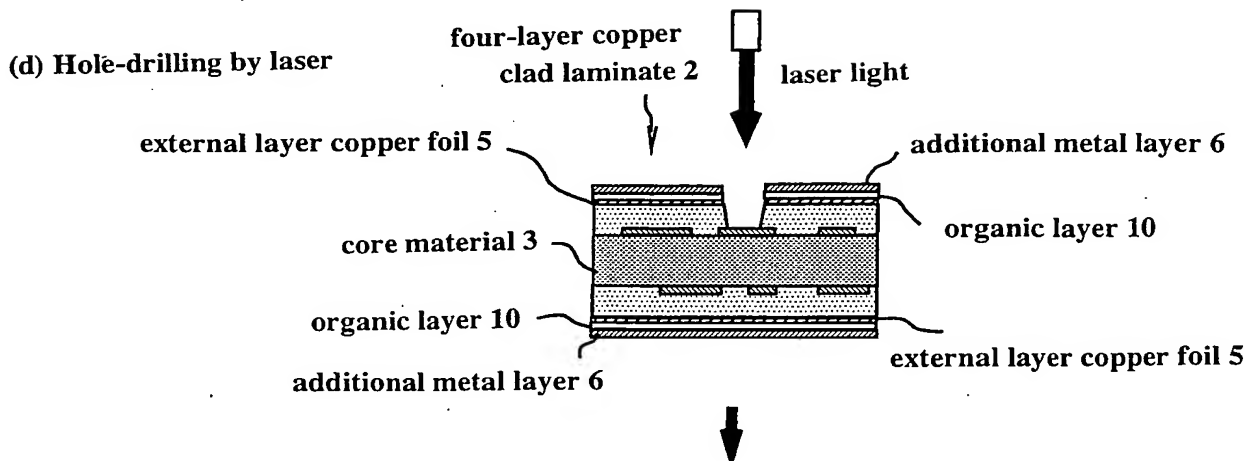
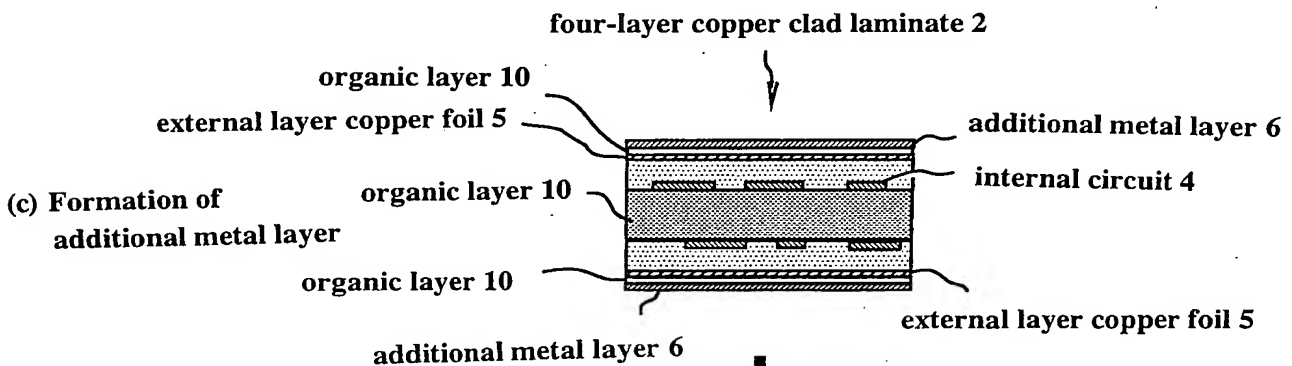
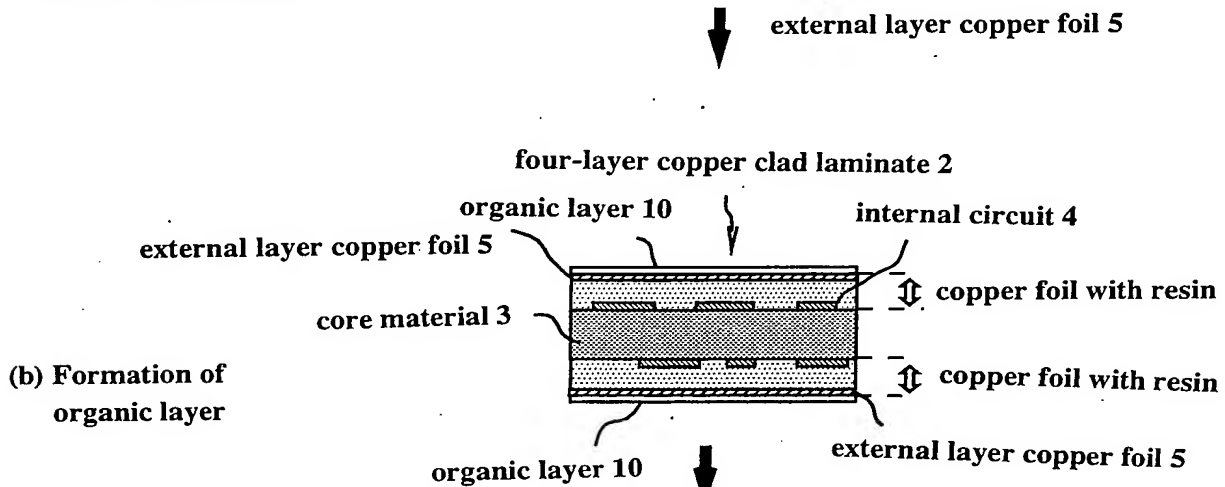
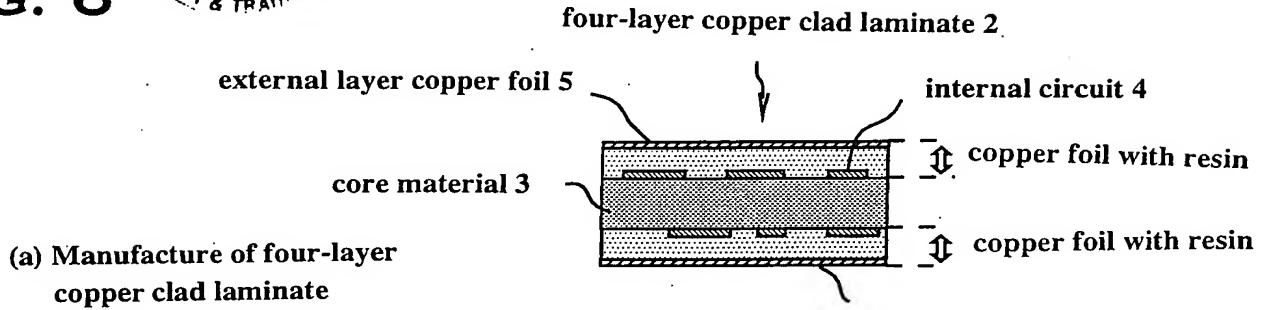
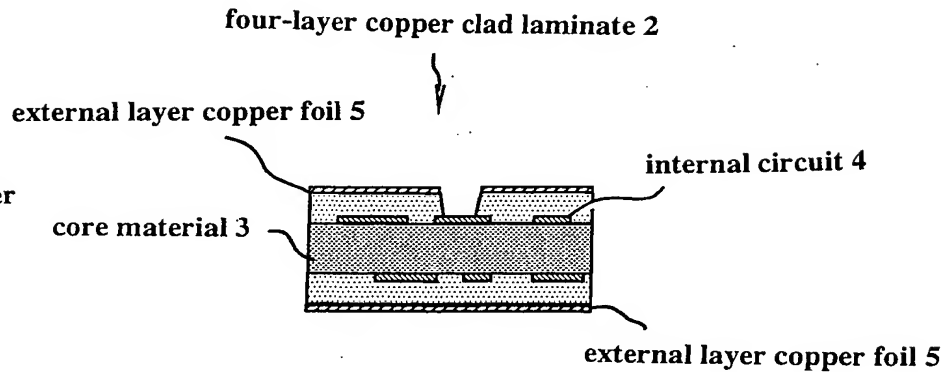


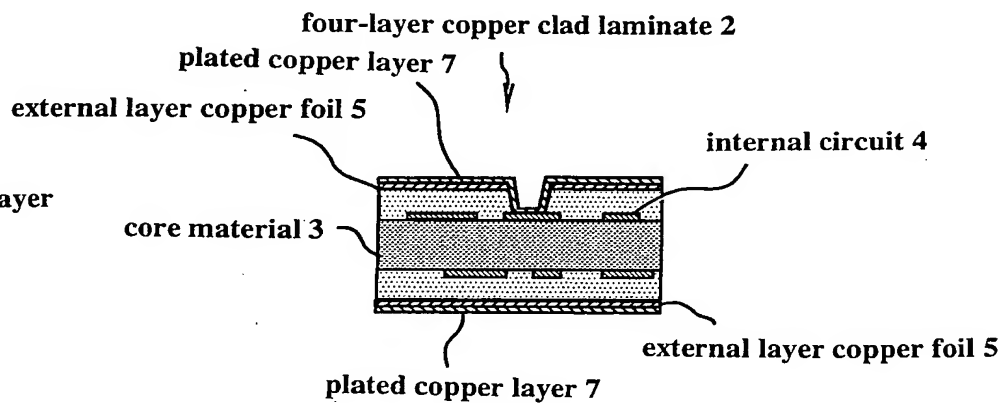
FIG. 7



(e) Peeling-off of
additional metal layer
and organic layer



(f) Formation of
plated copper layer



(g) Formation of
etching resist layer

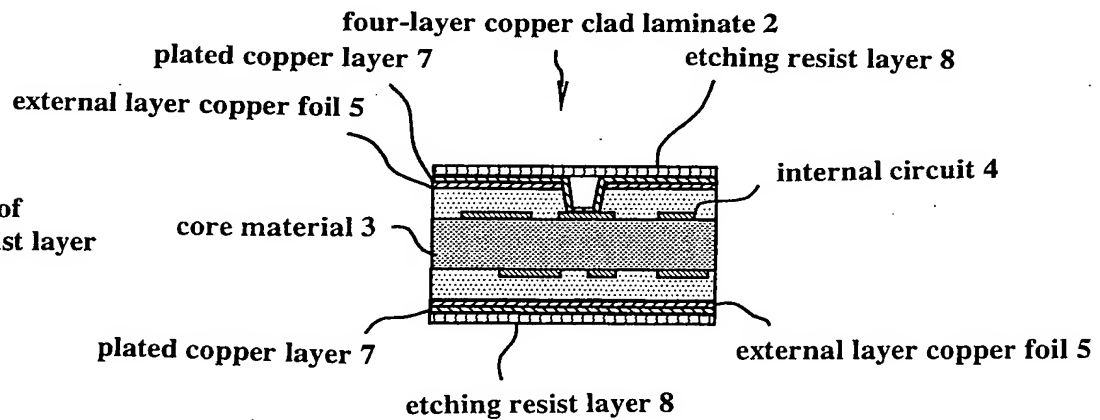
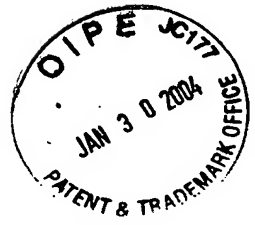
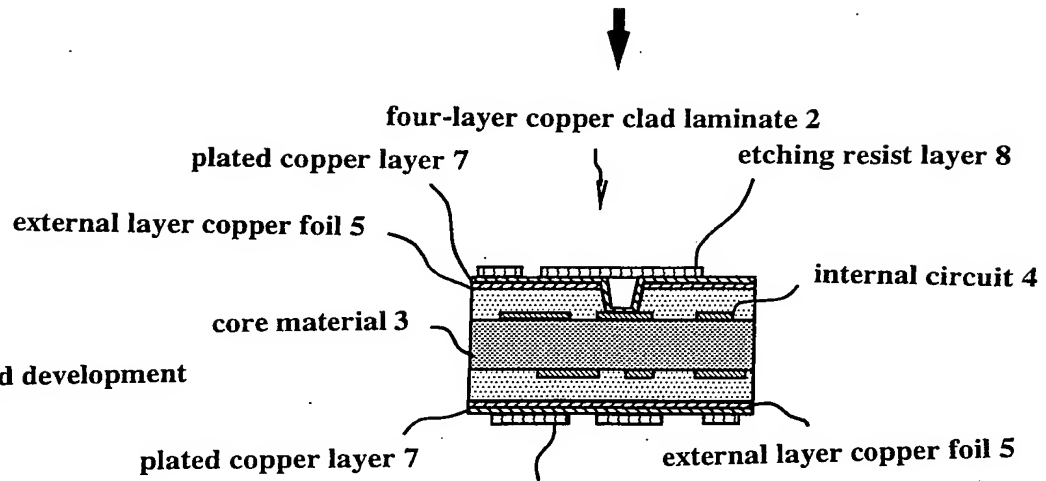


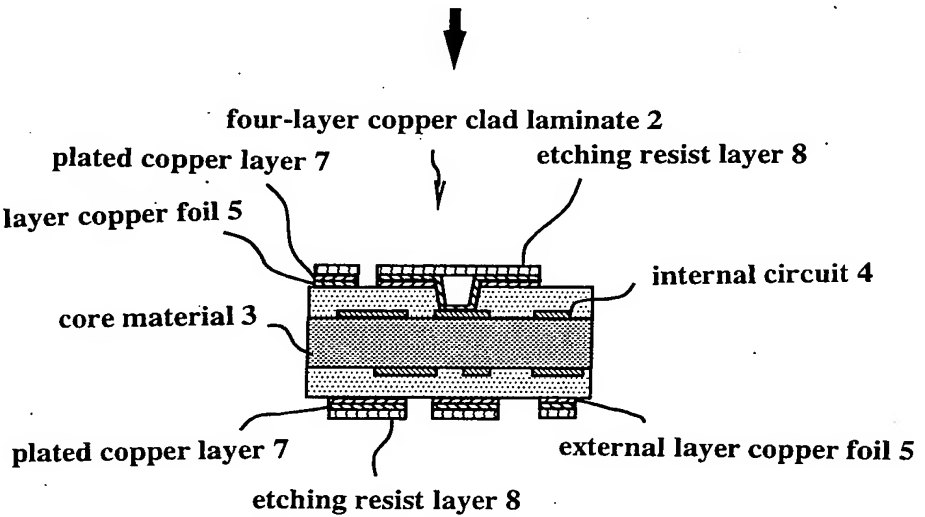
FIG. 8



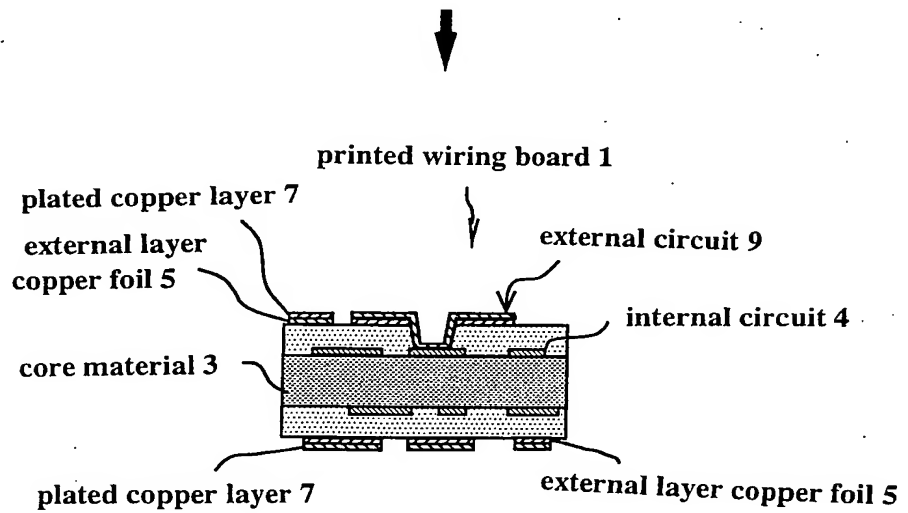
(h) Exposure and development



(i) Formation of a circuit through etching



(j) Peeling-off of etching resist layer



printed wiring board 1

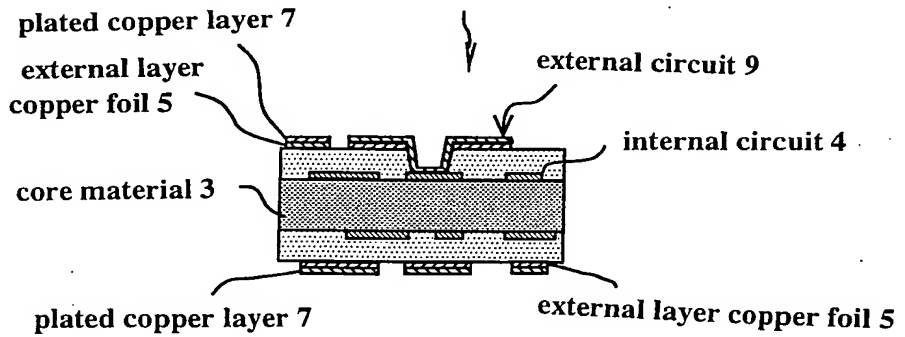


FIG. 9

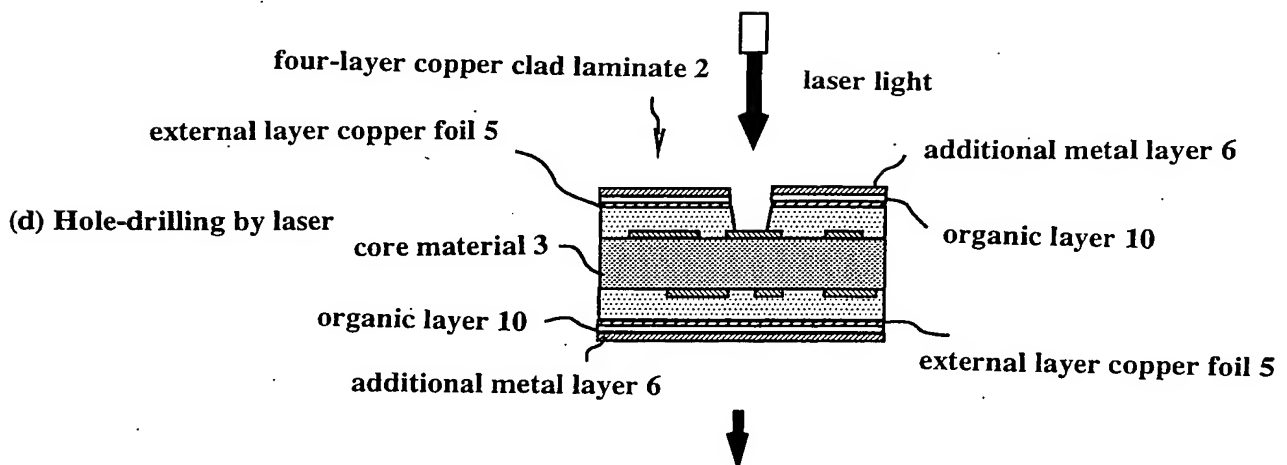
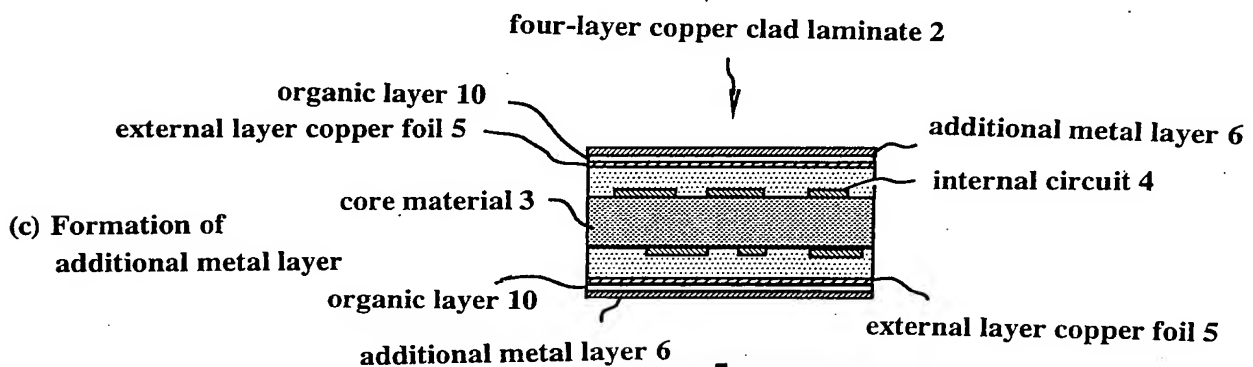
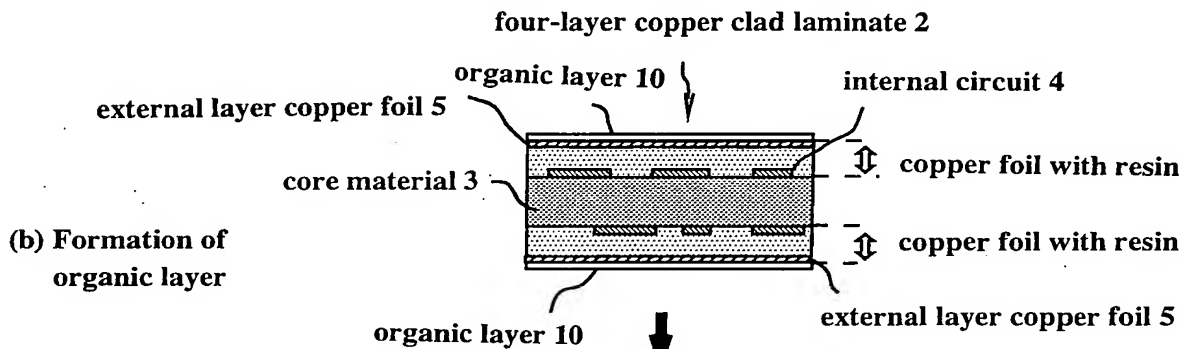
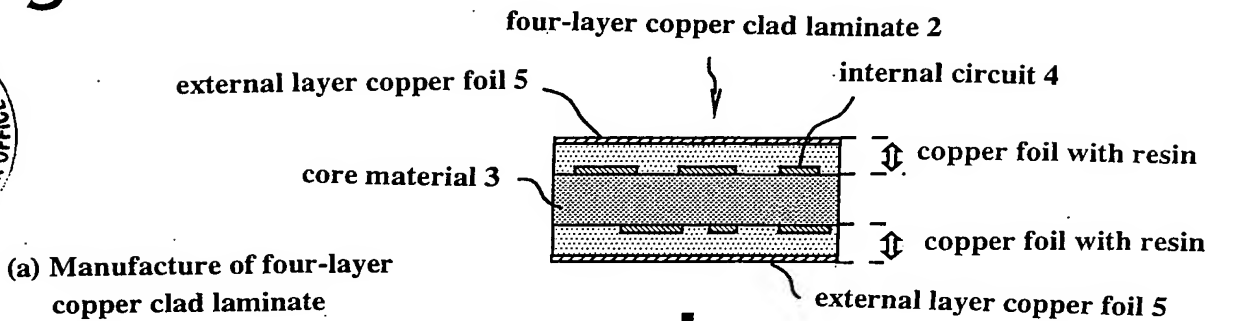
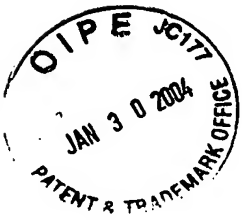
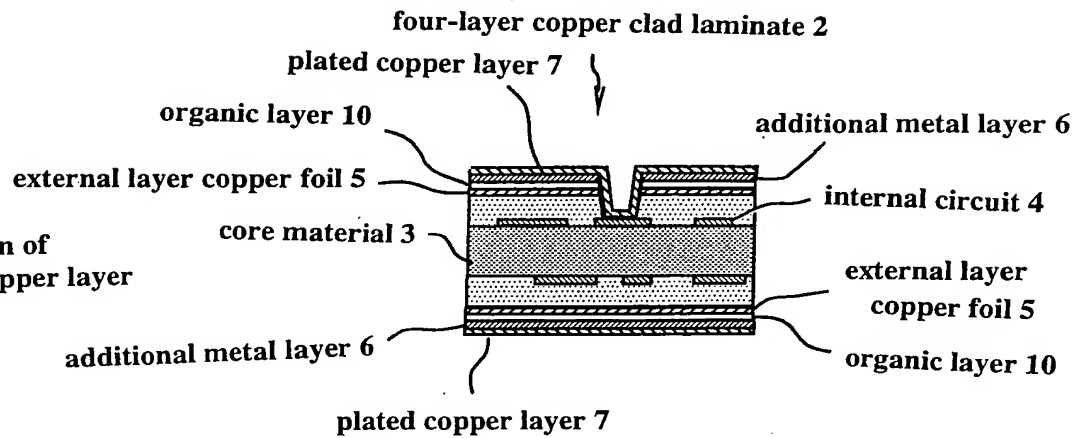


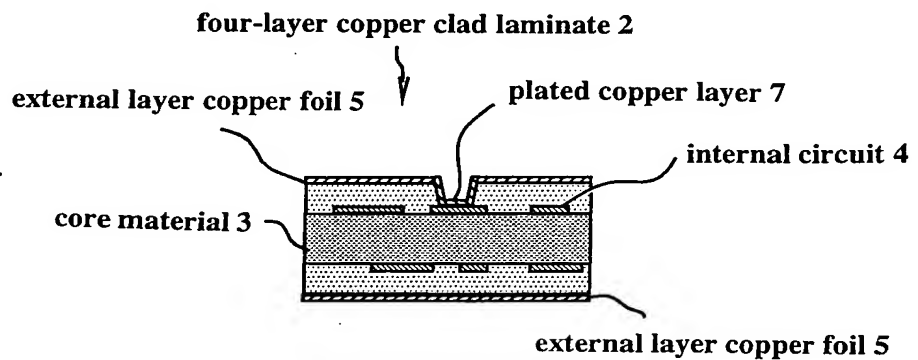
FIG. 10



(e) Formation of
 plated copper layer



(f) Peeling-off of
 additional metal layer
 and organic layer



(g) Formation of
 etching resist layer

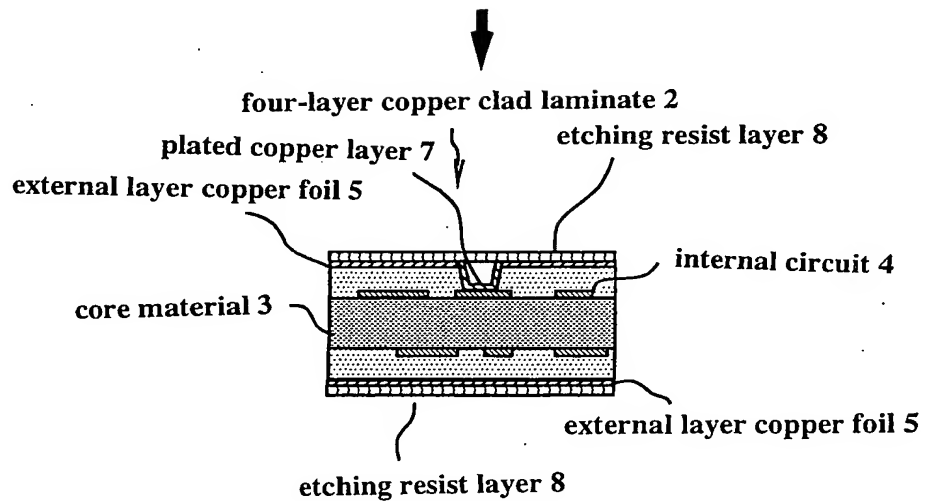
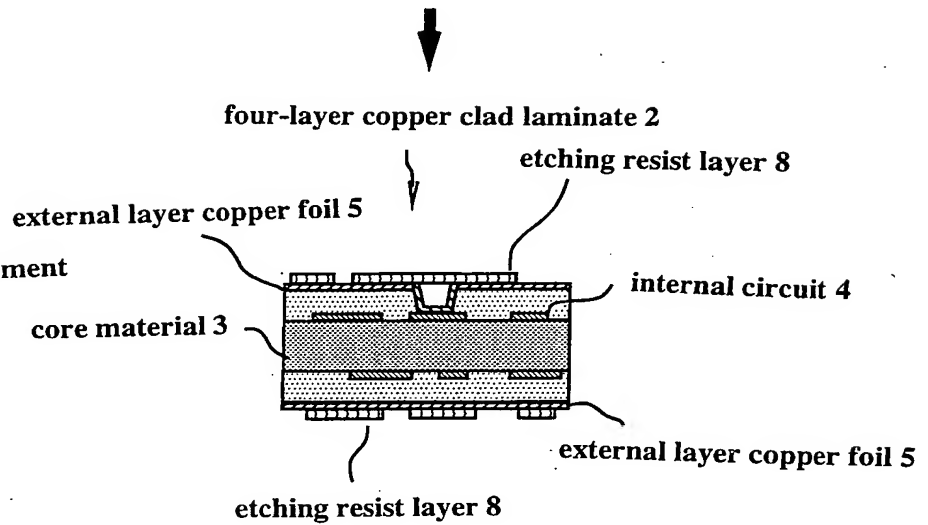


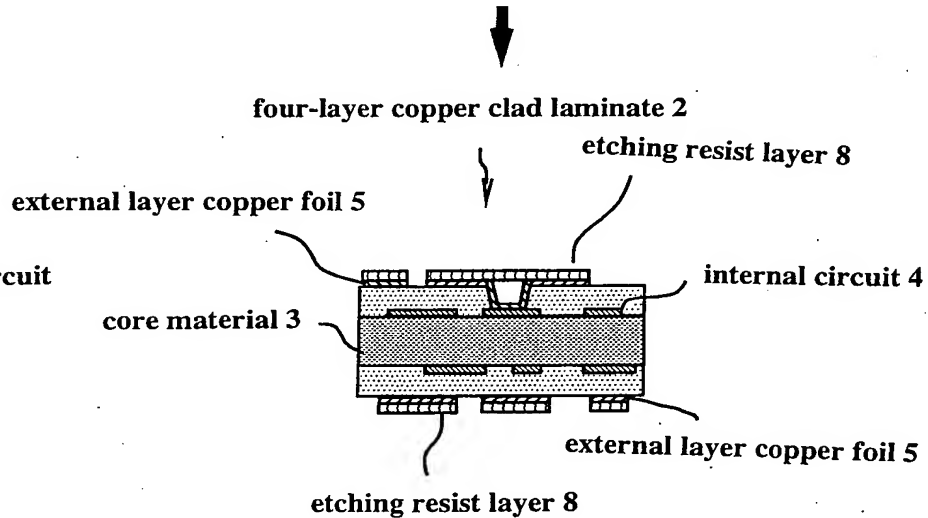
FIG. 11



(h) Exposure and development



(i) Formation of a circuit through etching



printed wiring board 1

(j) Peeling-off of etching resist layer

